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Fax

Page 1 of 17

Urgent

Confidential

Date: June 6, 2005

To:	**Fax:**	**Art Unit:**
Examiner: Steven HD Nguyen USPTO	(703) 872-9306	2665

From:	**Fax:**	**M/S:**
Stuart A. Whittington Intel Corporation	480-715-7738	

Subject: Application No.: 08/766,895 Docket #: 42390P3991
Filed: 12/13/1996 Inventor: Dunning et al.

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Lisa M. Hopkinson **Date:** June 6, 2005 Lisa M Hopkinson

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Fax Cover Sheet (1 page)
Transmittal Form (1 page)
Fee Transmittal (1 page submitted in duplicate)
Amended Brief on Appeal (13 pages including Appendix A)

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TRANSMITTAL FORM

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Total Number of Pages in This Submission: 17

Application Number	09/756,639
Filing Date	1/213/1998
First Named Inventor	David S. Dunning
Art Unit	2666
Examiner Name	NGUYEN, Steven HD
Attorney Docket Number	42390P3991

ENCLOSURES (Check all that apply)

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavit/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please identify below):
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Remarks

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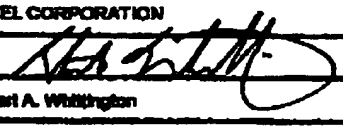
Signature			
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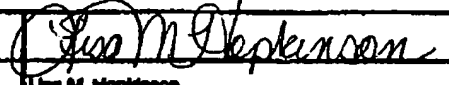
Signature			
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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 600.00

Complete if Known	
Application Number	09/766,895
Filing Date	12/13/1996
First Named Inventor	David S. Dunning
Examiner Name	Steven HD Nguyen
Art Unit	2665
Attorney Docket No.	42390P3991

METHOD OF PAYMENT (check all that apply)

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☑ Deposit Account Deposit Account Number: 50-0221 Deposit Account Name: Intel Corporation

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	Fee ($)	Fee Paid ($)
	_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	_____
Other (e.g., late filing surcharge): 41.20(b)(2) - 1402 - Filing a Brief in Support of an Appeal	$500

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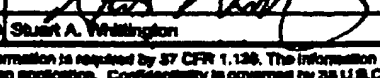
Signature		Registration No. (Attorney/Agent) 45,215	Telephone 480-715-3695
Name (Print/Type)	Stuart A. Whittington		Date June 6, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Dunning et al. Atty. Docket No: 42390.P3991

Appln. No.: 08/766,895 Group Art Unit: 2665

Filed: December 13, 1996 Examiner: Nguyen, Steven H D

Title: METHOD AND APPARATUS FOR ROUTING ENCODED SIGNALS THROUGH A NETWORK

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BRIEF ON APPEAL

In response to the Advisory Action dated February 25, 2005 and pursuant to Appellant's Notice of Appeal filed on April 4, 2005, Appellant presents this Brief and fee under 37 C.F.R. § 1.17(c) in appeal of the Final Rejection dated November 2, 2004.

I. REAL PARTY IN INTEREST.

Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES.

There are no related appeals or interferences before the Board of Patent Appeals and Interferences known to Appellant, the Appellant's legal representatives, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS.

Claims 1-27 are pending in the application. Claims 1-27 stand finally rejected and are the claims subject to this appeal as are reproduced in Appendix A.

IV. STATUS OF AMENDMENTS.

No amendments have been filed after the Final Office Action dated November 2, 2004.

V. SUMMARY OF CLAIMED SUBJECT MATTER.

Simply stated and generally speaking, in one embodiment of Appellant's invention a method for routing encoded signals through a network is provided. The encoded signals are in a packed that may include a header which may be received and decoded by a switch (e.g., switch 140 in Fig. 1). At least a portion of the header may include encoded binary digital signals specifying a route through the network for the packet to navigate through the network. The switch may be able to determine the routing without decoding the header portion. More specifically, rather than decoding bits in a header that provides a switch information on how to route a packet to a destination port and then re-encode those bits, Appellant's embodiment provides a technique where a bit patter is chosen for the header so that when the bit pattern is encoded, it directly provides information regarding routing the packet through the network in its encoded form. (See pg. 10, ll. 3-10 of Appellant's specification).

Therefore, in this particular embodiment of Appellant's invention, the encoded binary digital signals specify a route through the network without having to decode the encoded binary

digital signals. This may be accomplished using a look-up table in a route unit or router, for example. (Pg. 10, ll. 10-13).

Fig. 2 provides an example of how a packet may be arranged in accordance with one embodiment of Appellant's invention. As shown, a packet may include a destination address as part of a header 310, a trailer 33 for use in cyclical redundancy checking (CRC) and a payload 320. The payload may include the data or binary digital signals being transferred. (Pg. 8, ll. 16-20).

By way of example, Appellants claim 1 recites:

A method of routing a packet (e.g., packet shown in Fig. 2) *of binary digital signals through a network, said method comprising:*

receiving at a switch (e.g., switch 140) *in said network the packet of binary digital signals as encoded binary digital signals including a bit pattern* (e.g., bits in header 310) *chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form; and*

copying said bit pattern, at least for decoding.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL[1].

The sole issue for consideration on this appeal is:

A. Whether claims 1-27 are properly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,442,474 to Huang et al. (hereinafter "Huang").

VII. ARGUMENT.

A. THE CLAIMS ARE NOT ANTICIPATED BY HUANG.

Claims 1-27 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,442,474 ("Huang"). For the reasons that follow, Appellant respectfully requests this rejection be overturned.

As is well-established, in order to establish a *prima facie* case of anticipation, the cited prior art must teach or suggest every limitation of the claims being rejected. Therefore, if even one claim element or limitation is missing from the cited prior art, a *prima facie* case is not established.

It is respectfully asserted that, as one example, Huang fails to teach or suggest a method where binary digital signals are encoded to include a bit pattern selected so that it directly provides information regarding routing the packet through the network in its encoded form (e.g., Appellants **claim 1**).

This case has previously been before this Court on the same prior art grounds. (See Appeal No. 2003-0206 Decision). In its earlier decision, this Court noted that the Examiner's

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rationale regarding header bits was incorrect but affirmed the rejection on the Examiner's second rationale regarding the routing bits as Appellant did not address or rebut this issue in its previous appeal[2]. (Id at pgs. 7-9).

Thus the issue on this second appeal is whether Huang's router bits Ao-Do (Huang col. 6, ll. 14-31) read on Appellant's claims; Appellant respectfully submits they do not.

Huang discloses routing bits for each data packet A, B, C and D designated by subscript o. (Col. 3, ll. 56-57). These routing bits are used for de-multiplexing (i.e., separating a multi-channel signal into different channels) an N-channel optical signal consisting of multiplexed routing bits and data bits. (Col. 1, ll. 47-49; col. 6, ll. 23-24). In essence, each Huang packet includes routing bits Ao-Do which can be designated a binary logic value of 1 or 0. Depending on the binary value of routing bit signals Ao-Do, the exchange/bypass switch 170 of Huang can demultiplex the incoming signal into separate data signal paths. (Col. 6, ll. 28-31).

The crux of the rejection at hand is that the Examiner alleges routing bits Ao-Do are analogous to Appellant's claimed encoded binary digital signals having a bit pattern selected so that it directly provides information regarding routing the packet through the network in its encoded form.

Appellant concedes that Huang does have routing bits which are used to separate a multi-channel signal into respective communication paths (e.g., Fig. 5). However, Appellant does not

[2] This rational was never present in the Final Office Action but first set forth in the Examiner's Answer dated March 26, 2002.

believe routing bits Ao-Do are ever "encoded" or include any pattern nor does switch 500 route packets through a network in their encoded form. Instead, Huang routing bits Ao-Do simply have a pre-assigned binary logic state (i.e., 1 or 0) and the output of node 500 (Fig. 5) is only the data bits A1x-D1x (i.e., without routing bits Ao-Do there can be no routing of packets through the network in encoded form).

Appellant believes there is a fundamental misunderstanding of the instant invention. Appellant's invention is directed to methods and devices for routing encoded binary signals through a network without each network device having to independently decode the signals to know where they are to be routed; and thus they can be efficiently forwarded through the network in their encoded form. By way of contrast, Huang is directed to de-multiplexing a multi-channel signal by checking logic values of individual routing bits. Appellant submits Huang does not teach or suggest encoded binary signals or an encoded bit pattern.

Respectfully, Appellant believes Huang is not remotely related to the instantly claimed invention since encoding and decoding are not disclosed by Huang whatsoever. Accordingly, the additional limitation of *copying the bit pattern, at least for decoding*, which are recited in Applicant's claims 1 and 10 are also not disclosed or suggested by Huang.

Furthermore, independent **claims 10, 17, 22 and 25** all recite the limitation, that *when the bit pattern is encoded it directly provides information regarding routing of the packet routing the packet through the network in its encoded form without decoding.* Again, since Huang does not

mention or suggest any type of encoding or decoding, it is respectfully submitted that Huang cannot anticipate these claims.

In the Final Office Action dated November 2, 2004, the Examiner alleges that "Huang discloses encoded binary signals by virtue of the routing bits being in binary form such as 0 and 1. (11/04/04 Final Office Action pg. 8). Appellant respectfully believes this interpretation is not reasonable and would not be the interpretation of one skilled in the art in view of the specification and existing prior art. All binary signals are necessarily in the form of 1s or 0s so given this overly broad interpretation, all binary signals would encoded binary signals. Respectfully, this interpretation entirely disregards the embodiments (and context) disclosed in Appellant's specification (see pg. 9, ll.14-15) as well as that known by one of ordinary skill in the art. There are many techniques for encoding binary signals, including for example Manchester encoding, as discussed in Appellant's specification.

In respect to **claim 10**, the Office Action alleges that Huang node 500 is analogous to Appellant's claimed switch. Here, Appellant specifically recites a bit pattern (e.g., a pattern of bits) chosen so that when the bit pattern is encoded, it directly provides information..... The Office Action alleges Huang routing bits are analogous to Appellant's bit pattern. However, there is no pattern or arrangement of Huang routing bits to indicate routing information, it is the logic value of the routing bits themselves that provide routing information in Huang. While there may be a plurality of routing bits in the N-channel stream (Fig. 2), their pattern or arrangement has no significance in the routing function.

Additional limitations, but not necessarily an exhaustive list, present in Appellant's claims which are not believed to be taught or disclosed by Huang include:

-decoding the copied encoded binary digital signals (claims 2 and 12)

-translating the deserialized and decoded binary digital signals (claim 4)

-said encoded binary digital signals... comprise and encoded destination address (claims 8 and 15)

-encoded binary digital signals comprise...signals specifying a route through the network if decoded (claims 9 and 16)

-switch adapted to serially copy the encoded binary digital signals (claim 11)

-encoded binary signals specifying route through network without decoding comprise a portion of the header of the packet (claims 18 and 23) (see Huang Fig. 2)

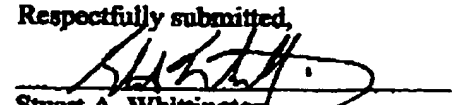
For all the foregoing reasons, Appellant respectfully submits that Huang does not anticipate claims 1-27 and the rejection thereof is requested to be overturned.

VIII. CONCLUSION.

It is respectfully submitted that in view of the foregoing all of the pending claims are patentable over the cited prior art references, alone or in any combination, and the Board is respectfully requested to overturn the rejections of record and allow this application to issue.

APPELLANT'S BRIEF
U.S. Appln. No. 08/766,895

Respectfully submitted,



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Date: June 6, 2005

APPENDIX A
(Claims on Appeal)

1. A method of routing a packet of binary digital signals through a network, said method comprising:

receiving at a switch in said network the packet of binary digital signals as encoded binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form; and

copying said bit pattern, at least for decoding.

2. The method of claim 1, and further comprising a step of decoding the copied encoded binary digital signals.

3. The method of claim 2, wherein the step of receiving the packet of binary digital signals comprises receiving the packet serially; and further comprising a step of deserializing the decoded binary digital signal.

4. The method of claim 3, and further comprising a step of translating the deserialized and decoded binary digital signals.

5. The method of claim 4, and further comprising a step of routing the received packet of binary digital signals in accordance with the translated binary digital signals.

6. The method of claim 5, wherein the step of routing comprises routing the packet of binary digital signals to another switch in the network.

7. The method of claim 5, wherein the step of routing comprises routing the packet of binary digital signals to its destination in the network.

APPENDIX A
(Claims on Appeal)

8. The method of claim 1, wherein said encoded binary digital signals used to route the packet through the network comprises and encoded destination address

9. The method of claim 1, wherein said encoded binary digital signals used to route the packet through the network comprise encoded binary digital signals specifying a route through the network if decoded.

10. An integrated circuit comprising: a switch adapted to receive a packet of binary digital signals as encoded binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form;

said switch being further adapted to copy the encoded binary digital signals including the bit pattern, at least for decoding.

11. The integrated circuit of claim 10, wherein said switch is further adapted to serially receive said packet and to serially copy the encoded binary digital signals used to route the packet through the network

12. The integrated circuit of claim 11, wherein said switch is further adapted to decode and deserialize of the copied encoded binary digital signals used to route the packet through the network.

13. The integrated circuit of claim 12, wherein said switch is further adapted to translate the decoded and deserialized binary digital signals.

14. The integrated circuit of claim 13, wherein the switch is coupled in the network, said switch being adapted to route the received packet of binary digital signals in accordance with the translated binary digital signals.

APPENDIX A
(Claims on Appeal)

15. The integrated circuit of claim 10, wherein the encoded binary digital signals used to route the packet through the network comprise an encoded destination address.

16. The integrated circuit of claim 10, wherein the encoded binary digital signals used to route the packet through the network comprise encoded binary digital signals specifying a route through the network if decoded.

17. A method of routing a packet of binary digital signals through a network, said method comprising:

receiving at a switch in the network the packet of binary digital signals as encoded binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form without decoding.

18. The method of claim 17, wherein said encoded binary digital signals specifying a route through the network without decoding comprises a portion of the header of the packet of binary digital signals.

19. The method of claim 17, further comprising a step of: routing the packet of binary digital signals in accordance with the encoded binary digital signals specifying a route through said network without decoding.

20. The method of claim 19, wherein the step of routing comprises routing the packet of binary digital signals to another switch in the network.

21. The method of claim 19, wherein the step of routing comprises routing the packet of binary digital signals to a destination in the network.

APPENDIX A
(Claims on Appeal)

22. An integrated circuit to receive a packet of binary digital signals, the packet of binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through a network in its encoded form without decoding.

23. The integrated circuit of claim 22, wherein said encoded binary digital signals comprises a portion of the header of the packet of binary digital signals.

24. The integrated circuit of claim 23, wherein said switch is coupled in the network, said switch being adapted to route the packet of binary digital signals in accordance with the encoded binary digital signals specifying a route through the network without decoding.

25. An integrated circuit comprising: a route unit adapted to produce binary digital signals to be included in a packet of binary digital signals that after encoding includes a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through a network in its encoded form without decoding.

26. The integrated circuit of claim 25, wherein said route unit is embodied in a network interface component (NIC).

27. The apparatus of claim 26, wherein said NIC is coupled to a switch, said switch being adapted to route the packet of binary digital signals through the network in accordance with the encoded binary digital signals specifying a route through the network without decoding.